A LOW NOISE NMOSFET WITH OVERLAID METAL GATE

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Abstract

A new MOSFET device structure which adopts a overlaid-metal over poly-Si gate is proposed for using in RF low-noise amplification. Measurement result shows the minimum noise figure as well as the noise resistance of overlaid-metal gate MOSFET (OMGMOS) are smaller then conventional MOSFET. The equivalent circuit model of this OMGMOS device is generated and compared to that of the conventional MOSFET with same physical geometry. It shows the better noise characteristic of OMGMOS is mainly due to the decrease of the gate resistance.

I. INTRODUCTION

The using of Si MOSFET to construct radio frequency circuits in the modern wireless communication system has received a great attention during the last few years due to the rapid progress of Si MOSFET. In the published literatures, many research works had demonstrated the quite good performance of the Si MOSFET low noise amplifiers operated at 1~2GHz [1][2]. However the previous mentioned papers proposed various design techniques for obtaining the best noise characteristics of the conventional MOSFET. In this paper, we will propose a new low-noise MOSFET device structure constructed by the commercial CMOS process but it has better noise characteristics for using in the microwave low-noise application. In the conventional Si MOSFET fabrication technology, the poly-Si gate is adopted to constructing a self-aligned structure to minimize the channel length. But the poly-Si has higher resistivity than the connection metal. According to the Pucel's equations[3], the minimum noise figure (F_{min}) and equivalent noise resistance (R_n) of FET are determined by the following euqations:

$$F_{min} = 1 + 2\frac{\omega C_{gs}}{g_m}[K_g\{K_r + g_m(R_s + R_g)\}]^{1/2} + 2(\frac{\omega C_{gs}}{g_m})^2[K_g g_m(R_g + R_s + K_c R_i)] \quad (1)$$

$$R_n = \frac{(R_s + R_g)T}{T_0} + \frac{K_r(1 + \omega^2 C_{gs}^2 R_i^2)}{g_m} \quad (2)$$

Where the F_{min} and R_n are both proportional to gate resistance (R_g). In the conventional MESFET, the T-type or the mushroom gate is used to decrease the gate resistance. For decreasing the gate resistance, we simply overlay a metal over poly-Si gate as shown in Figure 1 to improve the noise characteristic of the MOSFET. The measurement result shows that this new MOS structure indeed has a lower noise figure than the conventional one.

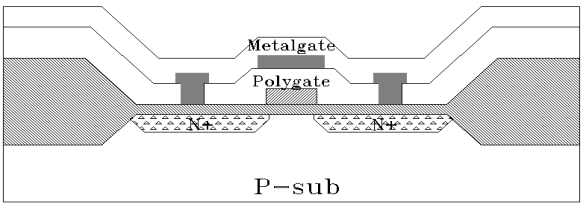

Figure 1 The cross section view of the overlaid-metal-gate MOSFET (OMGMOS)

II. PRACTICAL OMGMOS STRUCTURE

A 0.6um single-ploy-double-metal CMOS technology is adopted to fabricate the conventional MOSFET and overlaid-metal gate MOSFET

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(OMGMOS) on the same chip. As shown in Figure 1, the length of poly-Si gate is 0.6um. The overlaid metal gate is 0.8μm wide and placed directly above the poly-Si gate. The else structures are same as the conventional NMOS. The top view of OMGMOS is shown in Figure 2, which shows the way of connecting the metal gate and poly-Si gate outside the channel region via a connection plug. There are total 8 gate fingers used to constructing a 200μm device. The connection of different source regions are achieved by 2nd metal to cross over the poly-Si gate finger and the cross over area is keep as small as we can for minimizing the gate-to-source capacitance. After the devices are fabricated, the on-wafer measurement is performed to characterize their performance. Various bias conditions are tested, the both OMGMOS and conventional MOS have best noise characteristics under V_{DS}=3V and V_{GS}=2V bias condition. Under the above bias condition, the measurement result shows the maximum available gain of the OMGMOS has no great difference to the conventional MOSFET device in the commonly used personal communication bands. Comparing the measured noise characteristics of the OMGMOS and the conventional one, the minimum noise figure of the OMGMOS is about 1dB lower over 1 to 2 GHz range as shown in Figure 3. The noise resistance of the different devices are also depicted in Figure 3. It shows the OMGMOS also has smaller noise resistance. That implies the noise matching circuit of OMGMOS is easier to be designed and more insensitive to variation of components.

III. SMALL SIGNAL MODEL OF OMGMOS

The small signal model of OMGMOS same as that of conventional FET is shown in Figure 4. The device parameter extraction technique followed the work by Lee[4] is adopted to generate the equivalent circuit model of devices. The extracting technique started from determination of the extrinsic elements, which are R_s, R_g, R_d, L_s, L_g and L_d, by curve fitting the Z matrix of equivalent circuit model to the measured data. The curve fitting result is shown in Figure 5. Then a de-embedded Y matrix is generated by excluding the extrinsic elements. In the next step, the associated intrinsic device parameters of devices, such as C_{gs}, C_{gd}, C_{ds}, R_{ds}, transconductance (g_m) and delay time (τ), are obtained by solving equations derived from equating the de-embedded Y matrix and the Y matrix of the intrinsic equivalent circuit model [5].

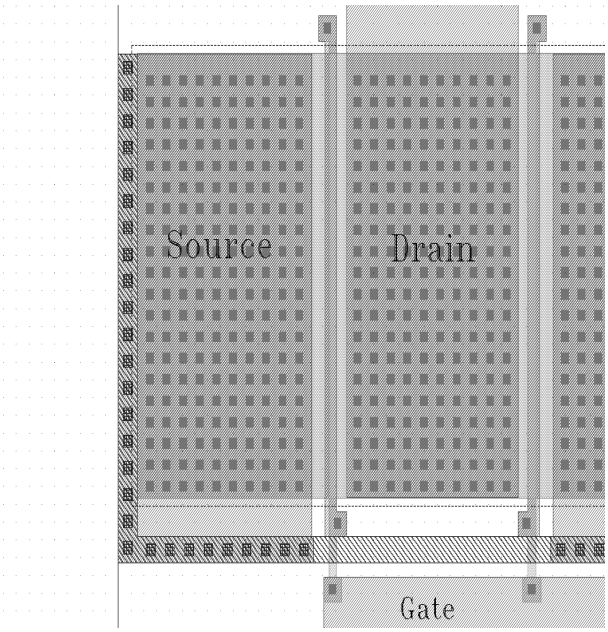


Figure 2 Top view of the OMGMOS

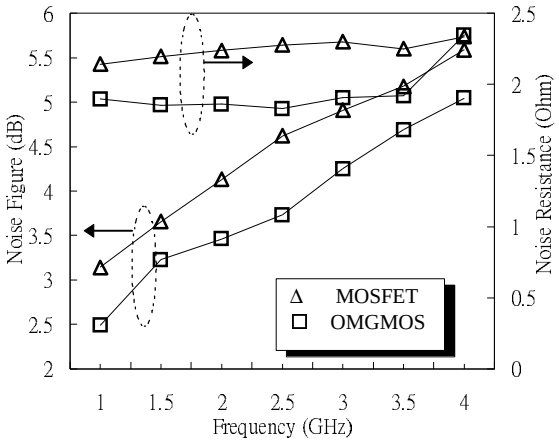


Figure 3 The comparison of minimum noise figure and noise resistance of the OMGMOS and conventional NMOS under the bias conditions with best noise performance.

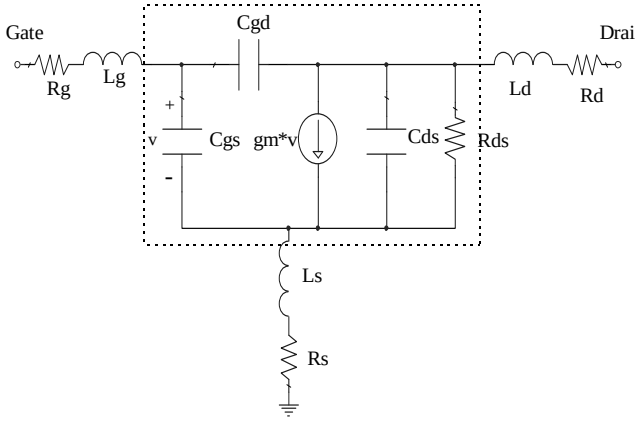
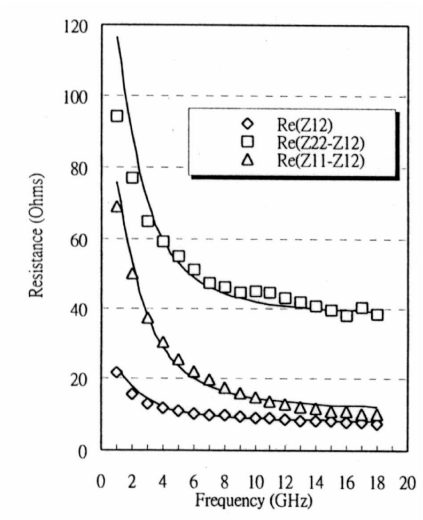


Figure 4. Equivalent circuit model of the OMGMOS



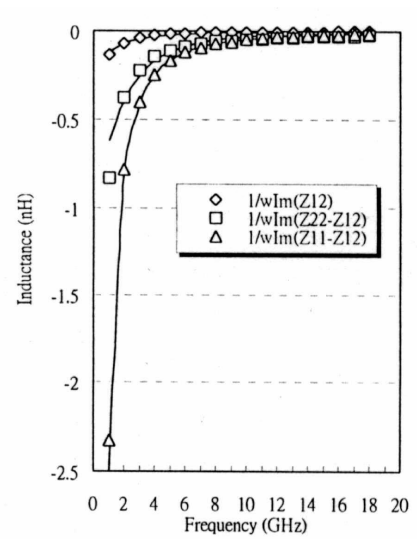


Figure 5 The curve fitting result of extracting the equivalent circuit model of OMGMOS.

The generated equivalent circuit model and the measurement result, which are in a quite good match, are superimposed in Figure 6. The same model extraction procedure is also used to generate the equivalent circuit model of the conventional MOS. Both the element values of the OMGMOS and the conventional MOS are listed in Table 1. As it shown, the gate resistor (R_g) is about one half of the conventional one, but the other parameters have no great difference. It proves that the using of overlaid metal gate can effectively reduce the gate resistance and thus improve the noise characteristics.

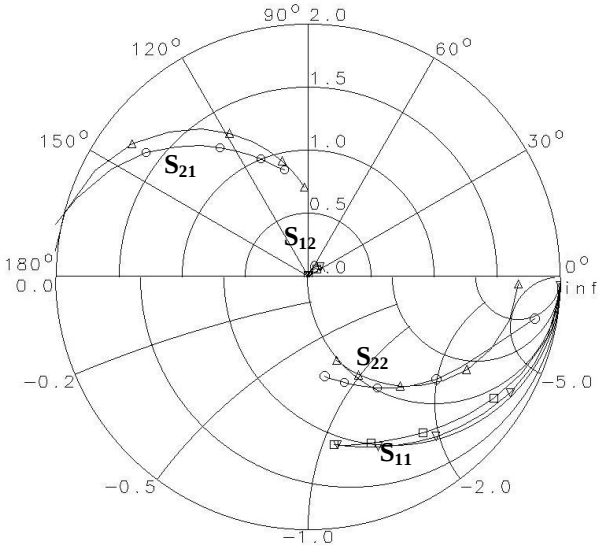


Figure 6 Comparison of the S-parameters of the equivalent circuit model and the measurement of OMGMOS under V_{DS}=3V, V_{GS}=2V bias condition.

IV. CONCLUSION

The operation frequency of the MOSFET device can be further pushed to higher frequency range by shrinking the gate length. However the minimizing of gate length cause the higher gate resistance. The proposed overlaid-metal-gate structure should be able to use in the future sub-micro MOSFET devices to effectively reduce the gate resistance without degrading the device performance.

Table 1. The equivalent circuit parameters of the OMGMOS and conventional MOSFET

		OMGMOS	MOSFET
Extrinsic Parameters	R_d	37.64	23.71
	R_s	7.86	6.70
	R_g	10.84	25.72
	L_d	0.087nH	0.13nH
	L_s	0.0208nH	0.022nH
	L_g	0.108nH	0.13nH
Intrinsic Parameters	C_{gs}	0.31pF	0.28pF
	C_{gd}	0.11pF	0.097pF
	C_{ds}	0.50pF	0.59pF
	R_{ds}	408.86	413.20
	g_{m0}	0.03S	0.027S
	τ	14.51p-sec	15p-sec

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